13. (Amended) A memory controller comprising:

a serial/parallel converter section for converting bit width a (where a is a positive number) of an input data signal into a width N times ($N \geq 4$) as long as a;

a first FIFO memory of a*N bits in width for storing temporarily the signal after it has been subjected to the serial/parallel conversion; and

a SDRAM having a capacity of a single frame for reading data at the same frequency as the input frequency of the input data after storing a predetermined quantity, a*N*L bits (where L is an integer), of the data into said first FIFO memory, and for storing the data read out from said first FIFO memory;

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a memory controller for reading from and writing into said SDRAM by driving successively as a single block;

a second FIFO memory having width a*N for reading from said SDRAM at the same frequency as the input data and for storing temporarily the data, such that, after storing data of a predetermined quantity 2*a*N*L into said second FIFO memory, the data is read at a frequency a half of the frequency of the input data, wherein

a continuous period of writing into and reading from said SDRAM is designed as an L cycle, a single time of continuous writing period and two times of continuous reading period are performed during a period N*L, an instruction period (including latency) instructing the memory necessary for performing continuous access to the SDRAM is the same as or shorter than a remaining period, N*L-3*L, so that a first FIFO size is set as a*N*L bits, and a second FIFO size is set as a*N*2*L bits.

15. (Amended) A memory controller comprising:

a serial/parallel converter section for converting bit width a (where a is a positive number) of an input data signal into an width M times ($M \geq 4$) as long as a;

a first FIFO memory of a*M bit width for storing temporarily the signal after it has been subjected to the serial/parallel conversion; and

a SDRAM having a capacity of a single frame for reading data at a frequency half of the input frequency of the input data after storing a predetermined quantity, a*M*L bits (where L is integer), of the data into said first FIFO memory, and for storing the data read out from said first FIFO memory;

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a memory controller for reading from and writing into said SDRAM by driving successively as a single block;

a second FIFO memory having width a*M for reading from said SDRAM at a frequency half of the frequency of the input data and for storing temporary the data, such that, after storing data of a predetermined quantity 2*a*M*L into said second FIPO memory, the data is read at a frequency a half of the frequency of the input data, wherein

a continuous period of writing into and reading from said SDRAM is designed as an L cycle, a single time of continuous writing period and two times of continuous reading period are performed during a period M*L, an instruction period (including latency) instructing the memory necessary for performing continuous access to the SDRAM is the same as or shorter than a remaining period, M*L-3*L, so that a speed of accessing said SDRAM is less than 1/2 of the data input speed.